Amendments to the Specification:

Please delete the superfluous duplicate heading entitled "Summary of Invention" immediately preceding paragraph [0010]. The heading was inadvertently included twice.

Please insert the heading "DETAILED DESCRIPTION OF THE INVENTION" between paragraphs [0200] and [0201].

Please replace paragraph [0001] with the following amended paragraph:

[0001] This application claims priority under 35 U.S.C. §119 to U.S. Provisional Patent Application Serial No. 60/450,133 entitled, "Systems and Methods for Upgradeable Scalable Switching and its Applications," filed on February 25, 2003, which is incorporated herein by reference in its entirety as if set forth in full. This application is also a continuation-in-part of U.S. Patent ~~Application Serial No. 09/897,263~~ No. 6,901,071, entitled "Row Upgrade for a Scalable Switching Network," ~~filed on July 2, 2001~~ issued on May 31, 2005, which is incorporated herein by reference in its entirety as if set forth in full. This application is also a continuation-in-part of U.S. Patent ~~Application Serial No. 10/074,174~~ No. 7,123,612 entitled, "Width Upgrade for a Scalable Switching Network," ~~filed on February 10, 2002~~ issued on October 17, 2006, which is incorporated herein by reference in its entirety as if set forth in full. This application is also a continuation-in-part of U.S. Patent ~~Application Serial No. 10/075,086~~ No. 7,075,942, entitled, "Fanout Upgrade for a Scalable Switching Network," ~~filed on February 10, 2002~~ issued on July 11, 2006, which is incorporated herein by reference in its entirety as if set forth in full.

Please replace paragraph [0011] with the following amended paragraph**:**

[0011] The redundant blocking compensated cyclic group (RBCCG) networks and hybrids form the basic building blocks of more elaborate switching networks. One such class of networks ~~are~~ is those formed from the Cartesian product of two switching networks. The Cartesian product of two switching networks can reduce the distance of the average connection between stages as compared to a similarly equipped "flat" switching network.

Please replace paragraph [0016] with the following amended paragraph**:**

[0016] The methods of implementing a scalable switching network with upgrade capabilities ~~is~~ are given with embodiments where software is used to assist a technician in upgrading a scalable switching network. In another embodiment, software coupled to indicator lights guide a technician in upgrading a scalable switching network. In another embodiment, a robotic instrument performs an upgrade using a patch panel. In another embodiment, switching elements are equipped with latched switches which enable a network to be laid out prior to an upgrade. In another embodiment, prefabricated interconnection can be inserted into a special interconnection box.

Please replace paragraph [0206] with the following amended paragraph**:**

[0206] In describing a switching network, several terms are used in this disclosure. In addressing any switching network, an external port to a switching network is a port of a switching element which is intended to be connected to a device not part of the switching network. Likewise, an internal port to a switching network is a port of a switching element which is intended to be connected to another switching element within. Similarly, an external connection is a connection between a switching element of the switching network and a potential external device and an internal connection is a connection between two or more switching elements within the switching network. For example, in **Fig. 6A**, switching network 200 comprises a plurality of switching elements 202, where some of the switching elements 202 have external ports 206 and 204 and internal ports 208. Conversely, some of the switching elements 202 only have internal ports. In this example, there ~~are~~ is a plurality of internal connections 210 and an external connection 212. An external port 204 need not be connected to an external device 214 as long as the port is intended to be connected to an external device. Furthermore, if the switching network is reconfigured, expanded or modified, an external port can be made converted to an internal port by simply connecting it to another switching element within the switching network. Likewise, an internal port can be made available to an external device thereby redefining the role to an external port. The distinction between internal and external is not intended to be a constraining property of the port, but merely as a logical allocation.

Please replace paragraph [0213] with the following amended paragraph:

[0213] On occasion, it is convenient to refer to a port as belonging to a stage or ISIC network, that is a port belongs to a stage if it belongs to a switching element belonging to the stage. A port belongs to an ISIC network if it is a top port and the top ports of the stage to which it belongs is coupled to the ISIC network. Conversely, if the port is a bottom port, it belongs to an ISIC network if the bottom ports of the stage to which it belongs is coupled to the ISIC network. One should not note by this convention a port need not be connected to belong to an ISIC network.

Please replace paragraph [0214] with the following amended paragraph:

[0214] It is often convenient to number these ports from 0 to $W \times F - 1$. Notationally, each switching element can be labeled as R(n,w) indicating it is w+1 switching elements from the leftmost switching element in stage n+1. **Fig. 9** depicts stage n+1 of switching elements, indicated as stage 400. In this example, F=3 and W=5 so the bottom and top ports for each switching element are numbered from 0 to 2, as indicated by 402 for the top ports and 404 for the bottom ports. If referring to the top ports and bottom ports of the stage, they are numbered from 0 to 14 as indicated by 406 and ~~408~~ 408, respectively. Mathematically, the relationship is a simple equation, for instance, top port 2 of switching element R(n,4) would be top port $4F$+2 of stage n. In discussion of higher dimensional switching networks, this concept can be extended to numbering of all ports of a two-dimensional stage ~~stage~~. For instance, bottom port (1,3) of switching element R(n,2,3) would be bottom port ($2F_1$+1,$3F_2$+3) of the ISIC network.

Please replace paragraph [0217] with the following amended paragraph:

[0217] One embodiment of a multistage switching network augmentation method is the insertion of ~~a~~ an extra stage. **Fig. 12** shows a network comprising a Banyan network 1002, an extra stage 1006 connected with ISIC network 1004, which in this case is identical to the ISIC network 1008 between the second and third stages of Banyan network. Since the Banyan network is functionally connected, the network depicted in **Fig. 12** is also functionally connected with fault tolerance derived from redundant paths much in the same way as an RBCCG switching network. It falls short however in that the type of stages are not interchangeable, and the addition of new stages can not necessarily be made arbitrarily. The addition of a stage in the

wrong position (or the wrong type of ISIC network) can yield a network which not only lacks fault tolerance, but may not be functionally connected.

Please replace paragraph [0218] with the following amended paragraph**:**

[0218] The shortcoming of arbitrary stage augmentation yields the following refinement to the multistage switching network augmentation method: the insertion of an extra stage with a CGISIC network. As depicted in **Fig. 11A**, a multistage switching network 1122 is connected through one set of its external ports 1124 to another stage of switching elements 1126, by ~~an~~ a CGISIC network 1128. In an alternate embodiment depicted in **Fig. 11B**, the same multistage switching network 1122 depicted in **Fig. 11A** is divided into two pieces 1142 and 1144, ISIC network 1150 is preserved with piece 1144. Equivalently, the multistage switching network could have been divided so ISIC network 1150 is preserved with piece 1142. A new stage 1146 is attached to piece 1142 through CGISIC network 1148, and to piece 1144 through ISIC 1150. Generally, the internal insertion depicted in **Fig. 11B** is less desirable than the external insertion depicted in **Fig. 11A** as an architectural design. Often times, the multistage switching network is available as a complete unit whereby the internal connections can not be broken. Furthermore, unlike the external insertion depicted in **Fig. 11A**, the connectivity of the network can be detrimentally impacted to the point of no longer being functionally connected, especially if the initial multistage switching network is a radix two network, whereas with an external insertion, the resulting network is guaranteed to be functionally connected if the initial multistage switching network is functionally connected. Furthermore, with an internal insertion, any calculation-based routing can be severely impacted, whereas with an external insertion calculation-based routing of the multistage switching network can be used in combination with the calculation-based routing of a CGISIC network described below.

Please replace paragraph [0221] with the following amended paragraph:

[0221] The first example, depicted in **Fig. 13A**, shows a 32-port switching network comprising a Banyan network 1102, an extra stage 1104 and a CGISIC network 1106. The second example, depicted in **Fig. 13B**, shows a 32-port switching network comprising a crossover network 1122, an extra stage 1124 and a CGISIC network 1126. The third example, depicted in **Fig. 13C**, shows a 32-port switching network comprising a delta network 1142, an

extra stage 1144 and a CGISIC network 1146. The fourth example, depicted in **Fig. 13D**, shows a 32-port switching network comprising a Banyan network 1162, an extra stage 1164 and an inverted (upside-down) CGISIC network 1166. It should be noted that the orientation of the ISIC network 1166 does not affect the positive properties of the hybrid architecture. The fifth example, depicted in **Fig. 13E**, shows a 32-port switching network comprising a Banyan network 1182, an extra stage 1184 and a CGISIC network 1186. This example differs from the example depicted in **Fig. 13A** in that the extra stage is attached to the top of the network rather than the bottom. It should be noted that whether the placement of the extra stage is at the top or bottom of the network does not affect the positive properties of the hybrid architecture. The sixth example, depicted in **Fig. 13F** shows a 32-port switching network comprising a Banyan network 1202, an extra stage 1204 and ~~an~~ a CGISIC network 1206 generated from a variant of the standard group generator. This network differs from that of **Fig. 13A** in that the ISIC network 1206 utilizes a different generator than that of CGISIC network 1106. The seventh example depicted in **Fig. 13G**, shows a 32-port switching network comprising a BOP network 1222, an extra stage 1224 and ~~an~~ a CGISIC network 1226 generated from a variant of the standard group generator. ISIC network 1226 uses the same generator as that of the ISIC network 1206.

Please replace paragraph [0223] with the following amended paragraph**:**

[0223] An extra stage augmentation of fixed radix switching networks yields networks whose width is constrained to a power of the radix which typically is the fanout of each switching element. For example, Figs. 13A-13G still have a width which is a power of two, although, they are no longer confined to a height which is radix-based logarithm of the ~~the~~ width (i.e. $\log_F W$). Additional methods to augment many of the traditional multistage switching network architectures are given in the forthcoming examples.

Please replace paragraph [0239] with the following amended paragraph**:**

[0239] Though described for RBCCG networks, the Cartesian product of two or more networks can be defined in much the same way. The Cartesian product of two networks of equal height is to take the Cartesian product of their respective interconnection mappings defining each ISIC network. As an example of this method, **Fig. 21A** depicts a balanced RBCCG network and **Fig. 21B** depicts a Banyan network. The mapping of the ISIC network of **Fig. 21A** is shown in

Fig. 22A. The mapping of the upper ISIC network of the Banyan network shown in **Fig. 21B** is shown in **Fig. 22B** and the mapping of the lower ISIC network is shown in **Fig. 22C**. The mapping of the Cartesian product of the two networks ~~are~~ is shown in **Fig. 22D** for the upper ISIC network and **Fig. 22E** for the lower ISIC network. For clarity sake, no additional diagrams or depictions are shown, but one of ordinary skill could easily render such a network.

Please replace paragraph [0246] with the following amended paragraph:

[0246] In one embodiment, the Banyan network shown in **Fig. 24A** with [[a]] 4 rows and 8 columns is overlaid on the balanced RBCCG network shown in **Fig. 24B** with 8 rows and 4 columns and fanout per switching element of 2, resulting in the overlaid switching network shown in **Fig. 24C**. In another embodiment, the Banyan network shown in **Fig. 24A** with 4 rows and 8 columns is overlaid on the switching network shown in **Fig. 24D** comprising three Banyan networks coupled through a common stage of switching elements having 8 rows and 4 columns and fanout per switching element of 2, resulting in the overlaid switching network shown in **Fig. 24E**.

Please replace paragraph [0251] with the following amended paragraph:

[0251] Furthermore, **Fig. 30A** and **Fig. 30B** further ~~illustrat~~ illustrate the advantages in improved latency and fault tolerance. **Fig. 30A** highlights the six paths from the two highlighted external ports that occur naturally as part of the IRIC networks flowing from top to bottom. **Fig. 30B** shows four additional paths which are shorter than the six "natural" paths. These four paths incorporate connections in the ICIC networks. The result is shorter latency options and additional paths. The added fault tolerance additionally facilitates the upgradeability of overlaid networks without disruption of service. Such upgrade methods are described below.

Please replace paragraph [0282] with the following amended paragraph:

[0282] There is no known investigation of the process of upgrading the fanout of Banyan networks. There are two likely reasons why such an upgrade path is undesirable. First, most implementations of switching networks using the Banyan architecture employ specific binary sorting algorithms to route traffic. Second, an upgrade of an n-stage 2^{n+1}-port binary network to an n-stage 2×3^n-port trinary network or n-stage 2×4^n-port quaternary network would entail an

exponential growth in the number of ports required. For example, the 3-stage networks discussed above would involve an upgrade from a 16-port binary network to a 54-port trinary network to possibly the 128-port quaternary network. For a 4-stage network, this upgrade path would progress from a 32-port binary network to a 162-port trinary network to a 512-port quaternary network. For a 5-stage network, this upgrade path would progress from a 64-port binary network to a 486-port trinary network to an astronomical 2048-port quaternary network. Given that these are among the smallest upgrade scenarios, it is likely there would be little need for such upgrades. However, with the methods disclosed below and in prior U.S. Patent ~~Application Serial No. 10/075,086~~ No. 7,075,942, such an upgrade can be performed if desired.

Please replace paragraph [0293] with the following amended paragraph**:**

[0293] At step 6116, all the ISIC networks are reconfigured, that is, they are rewired in accordance with the post-reconfiguration switching network or the intermediate reconfiguration switching network if the reconfiguration process involves a stage removal. During the rewiring step connections are described a broken, but in actuality it can be necessary to divert traffic away from the ports coupled to the connection. Often, the ports coupled to the connection can be shutdown or stopped. While decoupled from one port the connection can be moved to another port leaving the other end of the connection coupled to another port though the stage of the connection is that of being disconnected. Regardless the ~~the~~ physical requirements, the rewiring process at the high level is described in terms of breaking connections and establishing connections. Additional steps are given at a lower level description of the process.

Please replace paragraph [0323] with the following amended paragraph**:**

[0323] The first example is that of a stage upgrade, whereby an extra stage is added to a multistage switching network. **Fig. 52A** shows a pre-reconfiguration switching network, which is a 24-port 4 stage balanced RBCCG switching network with ISIC networks, 6552, 6554, and 6556. They are identical, but 6554 is drawn in an elongated manner for clarity when indicating where the new stage of switching elements is to be inserted. There are no external ports that need to be deactivated. There are no pre-connections that can be performed. The result of the network after the splicing step is shown in **Fig. 52B**, where ISIC network 6654 is systematically broken and reformed into new ISIC networks 6672 and 6676 in order to insert new stage 6674. After the

rewiring step, the switching network matches its post-reconfiguration architecture as shown in **Fig. 52C**, where ISIC network 6672 is rewired to ISIC network 6680. The result is a 24-port 5 stage balanced RBCCG switching network. A stage upgrade process was also set forth in prior application, U.S. Patent ~~Application Serial No. 09/897,263~~ No. 6,901,071.

Please replace paragraph [0364] with the following amended paragraph**:**

[0364] The relabeling phase begins by scanning bottom ports from left to right. Switching element R(*N*,2) is connected to R(2,2), but according to **Fig. 56**, bottom port 1 should be connected to R(2,2) instead of bottom port 0. The ~~connection~~ connections to those ports are swapped as shown in **Fig. 60A**.

Please replace paragraph [0365] with the following amended paragraph**:**

[0365] The relabeling phase continues by scanning bottom ports from left to right. Switching element R(*N*,2) is connected to R(2,3), but according to **Fig. 56**, bottom port 2 should be connected to R(2,3) instead of bottom port 0. The ~~connection~~ connections to those ports are swapped as shown in **Fig. 60B**.

Please replace paragraph [0366] with the following amended paragraph**:**

[0366] This completes the relabeling phase for ISIC network 7056. The ~~The~~ rewiring step continues by the following port section and resultant rewiring of the selected ports.

Please replace paragraph [0377] with the following amended paragraph**:**

[0377] This completes the rewiring of ISIC 7056. Since the remaining ISIC networks are identical and both are equally distant from the "middle" of the switching network, the choice is completely arbitrary. Since they are identical, [[a]] examples are given with and without the optional relabeling step. First, ISIC network 7058 is selected and is rewired without the benefit of relabeling.

Please replace paragraph [0397] with the following amended paragraph**:**

[0397] The relabeling phase begins by scanning bottom ports from left to right. Switching element R(0,1) is connected to R(1,0), but according to **Fig. 56**, bottom port 2 should

be connected to R(1,0) instead of bottom port 1. The ~~connection~~ connections to those ports are swapped as shown in **Fig. 62A**.

Please replace paragraph [0398] with the following amended paragraph**:**

[0398] The relabeling phase continues by scanning bottom ports from left to right. Switching element R(0,2) is connected to R(1,2), but according to **Fig. 56**, bottom port 1 should be connected to R(1,2) instead of bottom port 0. The ~~connection~~ connections to those ports are swapped as shown in **Fig. 62B**.

Please replace paragraph [0399] with the following amended paragraph**:**

[0399] The relabeling phase continues by scanning bottom ports from left to right. Switching element R(0,2) is connected to R(1,3), but according to **Fig. 56**, bottom port 2 should be connected to R(1,3) instead of bottom port 0. The ~~connection~~ connections to those ports are swapped as shown in **Fig. 62C**.

Please replace paragraph [0400] with the following amended paragraph**:**

[0400] The relabeling phase continues by scanning bottom ports from left to right. Switching element R(0,3) is connected to R(1,1), but according to **Fig. 56**, bottom port 2 should be connected to R(1,1) instead of bottom port 0. The ~~connection~~ connections to those ports are swapped as shown in **Fig. 62D**.

Please replace paragraph [0480] with the following amended paragraph**:**

[0480] This completes the relabeling ~~relabeling~~ phase for ISIC 7112. The upgrade process now continues with the port selection phase of the rewiring step.

Please replace paragraph [0553] with the following amended paragraph**:**

[0553] **Fig. 78** shows a 24-port 4 stage pre-reconfiguration balanced RBCCG multistage switching network 7200. In addition to a width upgrade by adding the column 7201 of switching elements R(*,4), the network is also reconfigured to an unbalanced RBCCG multistage switching network. **Fig. 79** shows the 30-port 4 stage post-reconfiguration unbalanced RBCCG multistage switching network, wherein the CGISIC networks used in **Fig. 79** are shifted variants of

balanced CGISIC networks. Since this is [[a]] an upgrade, no external ports are disconnected during this process.

Please replace paragraph [0625] with the following amended paragraph:

[0625] For clarity, the ISIC networks are omitted from the diagrams to follow, but should be assumed to included as part of the switching networks described. **Fig. 86A** shows an expansion by a single vertical slice analogous to a column expansion in ~~an~~ a one-dimensional RBCCG. This causes an increase in the number of switching elements in the x_1 direction. Though not shown, the same kind of expansion could also be implemented in the x_2 direction. **Fig. 86B** shows a more arbitrary width expansion where the W_1 width is expanded by one but the placements are completely arbitrary; similarly, this could be applied to expansion to the W_2 width. **Fig. 86C** shows an expansion in both the W_1 and W_2 widths using a method analogous to column upgrades. **Fig. 86D** shows an expansion in both the W_1 and W_2 widths, but in a more arbitrary fashion. In **Fig. 86A**, **Fig. 86B**, **Fig. 86C** and **Fig. 86D**, the ISIC networks are not shown to simplify the diagram and the new switching elements are highlighted by hatching.

Please replace paragraph [0631] with the following amended paragraph:

[0631] Since both the IRIC and ICIC networks require reconfiguration, one could simply perform a width upgrade, considering the overlaid network as multistage switching networks, with the rows as the stages and the IRIC networks as ISIC networks. Then, perform a stage upgrade, considering the overlaid network as a multistage switching network, with the columns as the stages and the ICIC networks as the ISIC networks. In either order as proscribed, the process set forth for reconfiguring a multistage switching ~~networks~~ network. In that regard, the stage upgrade is recommended to be performed first because typically a stage upgrade tends to increase redundancy in the switching network, while a width upgrade tends to decrease redundancy and increase throughput.

Please replace paragraph [0635] with the following amended paragraph:

[0635] A few additional examples of reconfiguration of overlaid switching networks ~~is~~ are given. **Fig. 89A** shows the same RBCCG network as in **Fig. 88A**. **Fig. 89B** shows the addition of new top and bottom ports to each switching element in preparation for a fanout

upgrade. **Fig. 89C** shows the forming of all connections, in accordance with the post-reconfiguration switching network, which can be made without breaking existing connections; specifically the rightmost top and bottom ports of the rightmost switching elements are connected to the adjacent row's switching element. Only the IRIC networks need to be rewired, so the step follows identically the rewiring step as set forth above. For simplicity's sake, the optional relabeling is not performed here. **Fig. 89D** shows the result of rewiring the IRIC network between row 1 and row 2. **Fig. 89E** shows the result of rewiring the IRIC network between row 0 and row 1. **Fig. 89F** shows the result of rewiring the row 2 and row 3. Upon connecting and activating the new external ports introduced by the upgrade so that traffic is allowed to flow through them, the upgrade process is completed. It should be noted that the switching element rows are numbered from the 0 to 3 with row 0 at the top.

Please replace paragraph [0648] with the following amended paragraph**:**

[0648] The technician can be directed through the upgrade or reconfiguration through the process described in **Fig. 94**. The order of operation can be determined by a computer configured to operate the process in **Fig. 94**. For example, the connection to be manipulated in the step "determine next connection to be established" can be determined by a computer with the pre-reconfiguration architecture and ~~post-reconfigurationarchitecture~~ post-reconfiguration architecture programmed. From those two switching networks and the current state of the present switching network, the computer can determine based on the reconfiguration process set forth above, the next connection to be established. Furthermore, this computer can be in communication with the switching network and can monitor whether the correct connection is made. In one embodiment, the computer can back a technician out of an erroneous connection being established or broken.

Please replace paragraph [0650] with the following amended paragraph**:**

[0650] In the previous embodiment of upgrade assistance, the technician performs a rather mechanical operation. Due to the length and perhaps tedium of such ~~an~~ a procedure, it can be desirable to replace the technician in the procedure with a robot.

Please replace paragraph [0655] with the following amended paragraph:

[0655] During normal operations, only the first set of ports of the latching switches are connected to the other first set of ports of latching switches corresponding to other routers in such a fashion as to implemented the interconnection networks of the scalable switching architectures described. Though not required, these connections could be ~~implement~~ implemented through the use of a patch panel as described above. During this normal operation, the second set of ports on all the latching switches are all idle and need not have any connections to them.

Please replace paragraph [0657] with the following amended paragraph:

[0657] **Fig. 95A** depicts a pre-upgrade picture where router 9600 is connected through a latching switch 9602, through a connection 9604, to another latching switch 9606 to router 9608. ~~Supposed~~ Suppose during the upgrade process router 9600 should be connected to router 9610, then the second ports on latching switch 9602 and 9612 should be connected. When it is necessary to make ~~the make~~ this connection change, latching switch 9602 is thrown to break connection 9604 and latching switch 9612 is thrown to establish the new connection. It should be noted that now the port connected to latching switch 9606 is now broken as a result, but is presumably repaired later in the upgrade process. **Fig. 95B** depicts ~~an~~ a post-upgrade picture when router 9600 is connected to 9610.

Please replace paragraph [0674] with the following amended paragraph:

[0674] Traditionally, the Add / Drop multiplexers are circuit based and not packet based. A new generation of packet based Add/Drop multiplexers is being developed which combine the functionality of a circuit based Add/Drop multiplexer and a packet based router. A RBCCG network can also be used to accomplish this. Each column of routers of an RBCCG network can be located at different CLEC node. The connections from the top of the top column router and the bottom of the bottom column router are connected to either an access provider, a communication provider, a content provider, or a service provider. The connections from the internal column routers are either connected to other routers in the column are remotely connected by the CLEC to the internal column routers associated with other nodes. The RBCCG

routers thus separate the local traffic from the CLEC traffic and also help route the packets to their final destination.

Please replace paragraph [0688] with the following amended paragraph**:**

[0688] While certain embodiments of the inventions have been described above, it will be understood that the embodiments described are by way of example only. Accordingly, the inventions should not be limited based on the described embodiments. ~~For example, while embodiments involving a forklift were described above, it should be clear that the systems and methods described herein apply equally to embodiments for tracking a wide range of vehicles and items.~~ Thus, the scope of the inventions described herein should only be limited in light of the claims that follow when taken in conjunction with the above description and accompanying drawings.